

MIRAC2: a mid-infrared array camera for astronomy

William F. Hoffmann^a, Joseph L. Hora^b, Giovanni G. Fazio^b,
Lynne K. Deutsch^c, Aditya Dayal^d

^aSteward Observatory, University of Arizona

^bHarvard-Smithsonian Center for Astrophysics

^cAstronomy Department, Boston University

^dJet Propulsion Laboratory, Cal Tech

ABSTRACT

MIRAC2 was built for ground-based astronomy at Steward Observatory, University of Arizona and Harvard-Smithsonian Center for Astrophysics. It utilizes a Rockwell HF-16 128x128 arsenic-doped silicon blocked-impurity-band (BIB) hybrid array with a wavelength range of 2 to 28 μm operating in a liquid helium-cooled cryostat at 5 K.

Reflective optics, and externally actuated detector and pupil slides provide a variety of magnification and focal ratio settings without opening the cryostat. Nominal settings at the NASA IRTF and UKIRT give diffraction-limited imaging with .34 and .27 arcsec/pixel, respectively. The sensitivity on the IRTF at 11.7 μm , 10% bandwidth filter, chop-nod, source in one beam, 1 sigma, one minute total time is 25 mJy/arcsec surface brightness and 43 mJy point source.

Keywords: astronomy, BIB, camera, infrared, instrumentation, mirac

1. CAMERA DESIGN

MIRAC2 is an upgrade of MIRAC1, which was built by the University of Arizona, Smithsonian Astrophysical Observatory, and Naval Research Laboratory in 1988-89 (Hora, 1991, Hoffmann *et. al.*, 1993). It used a Hughes 20x64 Si:As photoconductive 20 line readout array. The conversion to a Rockwell 128x128 array was carried out between February and July 1994 for NASA IRTF observations of the collision of the comet SL-9 with Jupiter (Orton, *et. al.* 1995, Walter, *et. al.*, 1996). It has since been used on the IRTF and UKIRT for observations of planetary nebula, star forming regions, young stellar objects, the galactic center, infrared bright galaxies, QSO's, and a variety of solar system objects (Dayal, *et. al.*, 1997, 1998, Friedson, *et. al.*, 1995, Jayawardhana, *et. al.*, 1996, Orton, *et. al.* 1996).

The camera cryostat, shown in Figure 1, is an extended Infrared Laboratories Inc. HD-3 dewar with rigid supports and 0.8 liter liquid nitrogen and 2.0 liter liquid helium capacities with hold times of 16 and 25 hours, respectively. The fill openings, vacuum valve, connectors, and actuators are all on the top or bottom plates for compactness and easy transportability. Radiation from the telescope enters the cryostat horizontally through a ZnSe or KRS-5 optically-polished window and thence through LN2 and LHe temperature baffles.

The optics module contains a reflecting flat and a reflecting off-axis tilted ellipsoid of 7.17 cm focal length, both gold coated. The ellipsoid produces an image of the telescope entrance pupil (the undersized secondary for an infrared optimized telescope) at a cold stop and an image of the telescope focal plane at the detector. The cold stop is on an externally controlled slide with five positions for f/15, f/16, f/32, f/36, and f/45 beams. The detector array is on an externally controlled slide providing a range of magnification from 0.28 to 0.56. The parameters for several telescopes are given in Table 1. Two filter wheels operated with stepper motors and ferro-fluidic feed-throughs provide for a Circular Variable Filter (CVF) and 19 filter positions. The CVF and filter characteristics are given in Table 2. The 2.2 μm filter, for which the camera sensitivity is low, is used primarily for alignment, focus, and finding sources. The 4.8 μm filter, although considerably less sensitivity than a camera with an InSb detector is occasionally used for astronomical observations for direct comparison with longer wavelengths.

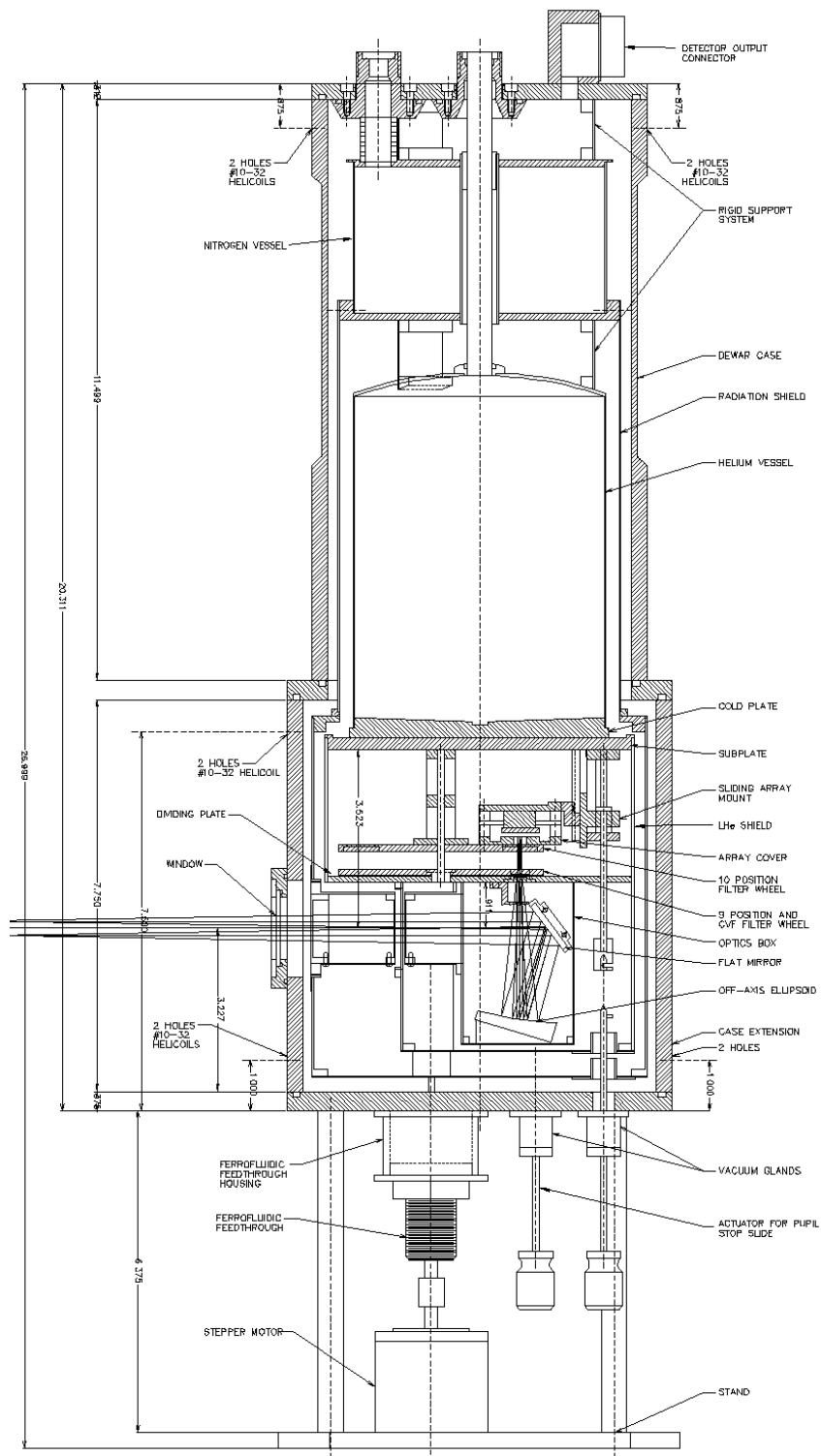


Figure 1. MIRAC Cryostat and optics.

The MIRAC2 camera electronics consist of six main units: power supply, located remotely, normally in the telescope control room, bias supply amplifiers, digital controller board, signal processors (16 with two on each of 8 boards), preamplifiers (16, one for each channel of the array), and temperature controller. These items, with the exception of the remote power supply, are located in an enclosure 14 x 12.5 x 23 inches in size mounted directly onto the camera cryostat.

For suppression of pickup and cross-talk, the power supply unit contains 7 separate supplies, preamp, bias, clock, analog-to-digital converter (A/D), signal processor, digital, and temperature monitor. The supply

returns are connected together and to ground only at the cryostat, with the exception of the signal processor analog and A/D supplies which are connected at the A/D ground plane. A consequence of this approach is negligible pickup and cross-talk with the system noise equal to approximately 0.4 A/D least significant bits.

The bias supply unit provides 14 separate detector bias voltages. The voltage settings and currents for these are given in Table 3.

The controller board provides a 15 MHz master timing frequency, detector clocking via optical isolators, and the timing for the signal processors and data acquisition. It is a wire-wrap board with largely discrete CMOS components of 1988 vintage, highly flexible, but difficult to work with.

Each signal processor board processes two channels from the array. The two channels have their own input amplifier, a 2 MHz 12-bit A/D, and an output FIFO memory buffer and share a digital adder and memory for fast coadding. The FIFO memory outputs connect via a backplane bus to a fiber optic driver for data transfer to the PC.

The 16 preamplifiers provide the source current for each of the array output MOSFET source followers, a gain of 4 amplifier, and an offset to bring the array outputs into the +/- 2.5 volt range of the A/D's. The preamplifier gain is chosen to provide least-significant-bit resolution close to amplified array read noise. Because of the limited resolution of the 12-bit A/D, this results in the amplified output voltage range of the array (2.1 V at saturation to 4.45 V at zero flux) exceeding the 5 V A/D range. To accommodate this the preamplifier has three offset values, commandable from the camera PC, a low range which

Table 1 Magnification and Pixel Sizes

Nominal settings are in bold face type							
Telescope	Aperture (m)	Focal Ratio	Scale ("/mm)	Mag	Pix (arcsec)	Field (arcsec ²)	λ for Pix= $\lambda/2D$
S.O. 90 in	2.3	f/45	1.99	.28	.52	66	11.5
				.33	.43	55	9.6
				.41	.36	46	8
IRTF	3.0	f/36.8	1.87	.33	.41	53	12
				.41	.34	44	10
				.49	.28	35	8
UKIRT	3.75	f/36	1.53	.33	.33	42	12
				.41	.28	35	10
				.49	.22	28	8

Table 2 MIRAC Filters

Wavelength μm	λ_1 μm	λ_2 μm	$\delta\lambda$ μm	Bandwidth fraction
2.2	2.02	2.38	.35	.16
3.8	3.5	4.1	.61	.16
4.8	4.42	5.18	.77	.16
7.9	7.74	8.06	.32	.04
8.8	8.36	9.24	.88	.10
9.8	9.31	10.29	.98	.10
10.3	9.79	10.82	1.03	.10
10.6	8.11	13.09	4.98	.47
11.7	11.14	12.26	1.13	.10
12.5	11.9	13.07	1.16	.10
17.4	17.17	17.63	.45	.026
17.8	17.57	18.03	.46	.026
18	17.1	18.9	1.8	.10
20.6	19.9	21.3	1.4	.068
CVF				
7.6			.10	.013
8.8			.13	.014
10.0			.17	.017
12.5			.21	.017
14.5			.21	.014

includes zero flux, a medium range covering from array read noise to the maximum linear range of the array, and a high range which includes the array saturation level.

The temperature controller utilizes a temperature-sensing diode to monitor the detector stage temperature and a heater and feedback control circuit to control the temperature to a selectable value with a stability of a few milli-Kelvin degrees rms. The temperature is normally set between 5 K and 7 K.

A fiber optic cable operating at 1 Mword/sec (32 bits) provides the data and command link between the camera and a Spectrum Signal Processing Inc TMS320C30 digital signal processor (DSP) located in a 66 MHz Pentium PC. The DSP provides the interface to send commands to the camera which set parameters and initiate data taking and to accept, format, and coadd data from the camera and transfer images to the PC for display and disk storage. When data is taken by fast sky chopping with a telescope secondary chopper and/or slow sky subtraction with telescope nodding, images from the separate sky positions are coadded into separate DSP buffers and separately saved to disk.

The PC computer is programmed in Pascal operating under the MSDOS operating system. The entire system is pipe-lined so that images can be continuously acquired without dead time. The array can be read out at a rate of 1.06 msec per array-read, co-images transferred to the PC at a rate up to 17 msec per transfer, and chop-nod observations processed, displayed and saved to disk up to a rate of one observation per second.

2. ROCKWELL HF-16 SI:AS BIB OPERATION

MIRAC2 uses a Rockwell (now Boeing) high-flux Si:AS BIB 128 x 128 BIB array (HF-16) mounted on a 68-pin leadless chip carrier. The pixels are 75 x 75 μm and the array sensitive area 9.6 x 9.6 mm. The relative spectral response of the detector is shown in Figure 2. The detector is responsive from 2 to 30 μm with high sensitivity in the mid-infrared range, 8 to 28 μm .

The HF-16 is a hybrid array. That is, the detector material is “bump-bonded” to a silicon multiplexer readout chip with indium bumps on facing aluminum pads, one for each of the 16384 pixels. The readout chip contains a unit cell circuit for each of the pixels (Figure 3) plus 16 output MOSFET source-followers, a fast and a slow shift register, and switching MOSFETS. Current from the detector is integrated on capacitor C_{INT} and read out through a source follower. The capacitor is reset through a reset MOSFET. The detector input node is isolated from the integration capacitor by a direct-injection MOSFET, which allows a large linear output voltage swing across the integration capacitor without affecting detector bias.

The 16 output channels are interleaved on the array in a 2 column by 8 row block as shown in Figure 4. Each of the pixels in a block are read at the same time. The pixels are not reset at the read time, but rather the 8 blocks in the lower half of the array are reset together while the first two blocks in the upper half are read and

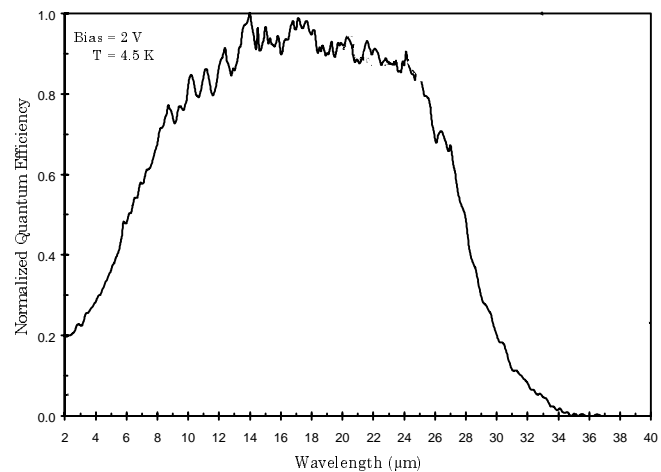


Figure 2. Relative spectral response of Si:As BIB detector (Stapelbroek, *et. al.*, 1995).

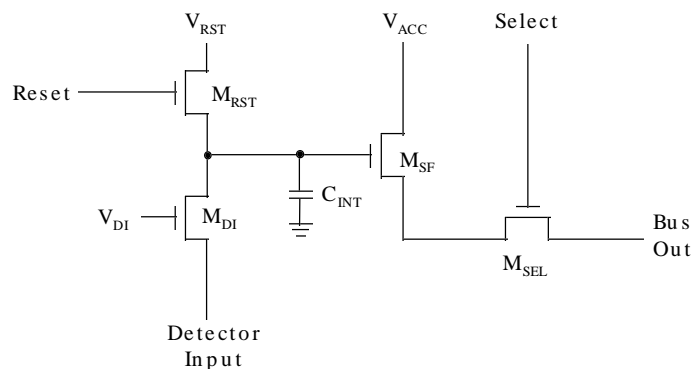


Figure 3. HF-16 multiplexer unit cell. Current from the detector flows through the direct injection MOSFET, M_{DI} , and is integrated on C_{INT} (Stapelbroek, *et. al.*, 1995).

the 8 blocks in the upper half reset while the first two blocks in the lower half of the next pair of columns are read. This makes it impossible to operate this array in a double sample mode, whereby each pixel is read both before and after resetting. Since this array is usually operated at high flux with the noise of each read dominated by photon-to-electron conversion shot noise, suppression of read 1/f noise by double sampling is not required. However, this resetting method necessitates a special approach to burst mode (fast read of the array after a slow integration period) as is discussed in Section 3. Conversions between channel (line) number, L, and block number, B, and column, C, and row, R, are given by:

$$R = \text{Int}[(L-1)/2] + 8 * \text{Mod}[(B-1),16] + 1$$

$$C = \text{Mod}[(L-1),2] + 2 * \text{Int}[(B-1)/16] + 1$$

$$L = 2 * \text{Mod}[(R-1),8] + \text{Mod}[(C-1),2] + 1$$

$$B = \text{Int}[(R-1)/8] + 16 * \text{Int}[(C-1)/2] + 1$$

Table 3 gives the input voltages and associated currents. “Cap” is the value of the shunt capacitor at the array circuit board used to suppress digital pickup in the bias lines. “Wire Ohms” is the resistance of the low thermal conductance wire from the connector at the cryostat top to the array board. “Series Ohms” is a series current-monitoring resistor on the bias amplifier board. VDI is the gate of the input charge injection MOSFET. DETS is the detector substrate. The detector bias is VDI - 1.0 - DETS. So with VDI 6.0 V and DETS 3.0 V, the detector bias is 2.0 V. VSOU is the voltage supplying the 30 Kohm series current-determining resistors for the output MOSFET source followers. The currents marked with an asterisk (*), are directly proportional to the photon flux on the array.

The HF-16 can be operated at room temperature to test the operation of the readout. At room temperature, the detector material has a low resistance and the operating point of the charge injection MOSFET changes. Operating at room temperature requires the following

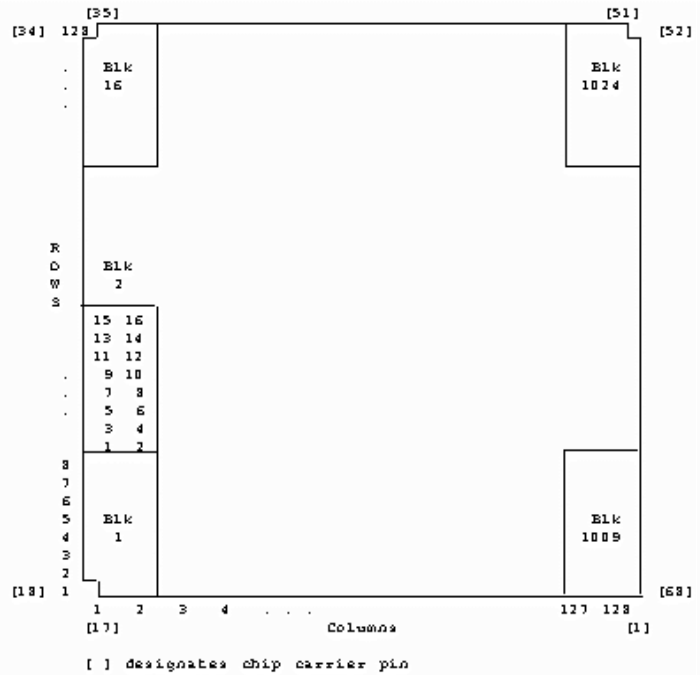


Figure 4. HF-16 multiplexer format. The 16 output lines multiplex the detector pixels in two-column by eight-row blocks, advancing in a series of sixteen block reads for each pair of columns, then advancing two columns and repeating this for a total number of 1024 block reads.

Table 3 Bias Inputs

Array Pin	Name	Cap nF	Wire Ohms	Volts	Current	Series Ohms
66	VACC	20	19.9	6.0	1.7 mA	5
52,67	CURS	20 to CGU/L	19.9	2.45	-1.7 mA	5
63	VTUB	20	20.6	9.5	0 μA	500
1,50	CURG	20	19.8	4.00	0 μA	50
24	VDDH	20	19.6	9.0	24 μA	500
62	VDI	40 to Dsub	21.1	6.0	0 μA	500
14,38	VDD	40	22.9	5.6	2.2 mA	5
53,54	VRST	40	19.7	6.9	14 μA *	500
60	DETG	20	19.9	5.0	.2 μA	500
55,59	VSSS	40	19.6	4.0	-7.6 μA	500
56,57	VDDS	40	19.8	9.0	7.6 μA	500
61	DETS	20	19.8	3.0	-15 μA*	500
65	VSSR	20	19.9	4.0	-2.2 μA	500
27	VSSH	20	19.7	4.0	-24 μA	500
Ext	VSOU			-1.6	-2.2 mA	5

actions. 1) Install a current limiting resistor (24.3 Kohm) in series with DSUB. 2) Increase DETS from 3.0 to about 4.95 V to reduce the bias across the detector to close to zero. 3) Adjust VDI for a reasonable range of linear operation as determined by an oscilloscope monitoring an array channel output. This normally requires changing VDI from 6.0 to 5.66 V. When this is done, one can observe the array outputs and DETS (hence detector) current change with a change in the DETS voltage.

VSOU can be adjusted to determine the current in the output MOSFET source follower, and hence its output impedance and resulting ability to drive the capacitance in the cable to the preamplifier. The higher the current, the lower the output impedance. However, this current should be kept minimal since the power dissipation of the output MOSFETs is the dominant source of self-heating of the array. The voltage difference between CURG and CURS determines the current through the integrating capacitor source follower, hence its frequency response.

The input, OVERRIDE, determines the length of the reset operation. With OVERRIDE low, the reset lasts two pixel times. With it high, the reset lasts two line times. We operate with OVERRIDE low for the highest integration duty cycle.

3. CAMERA TIMING AND OPERATION

The HF-16 requires three standard clocks and one non-standard one for burst mode. The standard clocks are fast clock (FSTCLK), which advances the array readout one block each transition, line Sync (LSYNC) which advances the readout two columns (16 blocks) each transition, and frame sync (FSYNC), which sets the shift registers at the beginning of the read cycle and controls the reset timing. These are shown in Figure 5.

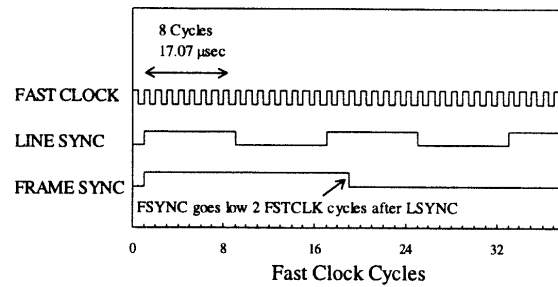


Figure 5. HF-16 clock timing. The readout advances one block of 16 pixels with each transition of Fast Clock. Each transition of Line Sync advances the readout two columns. Frame Sync resets the shift registers to the first block.

Each of the clocks runs between a low of 4.0 V (logical 0) and high of 9.0 V (logical 1). In MIRAC2 the rise and fall times of the clocks are about 20 nsec, characteristic of the CMOS chips used. LSYNC transitions occur at the rising edge of the FSTCLK wave form. The rising transition of FSYNC occurs at the rising edge of LSYNC. To provide proper synchronization of the shift registers and minimum reset time, FSYNC must be greater than one LSYNC cycle and less than two LSYNC cycles. To provide proper synchronization for the burst mode described below, we find that the falling edge of FSYNC should occur two FSTCLK cycles after one full LSYNC cycle.

As indicated in Section 2, the HF-16, with the reset occurring in groups of blocks after the reads, is not directly adapted to burst mode of operation where the array is rapidly read and reset and then charge accumulates for several read times before the next read-reset. Neither stopping FSYNC nor stopping all clocking results in proper resetting of the array. We have overcome this limitation by using the reset MOSFET switch drain bias, VDDR, as a clock to inhibit the reset during multi-read integration as shown in Figure 6. To achieve proper synchronization, the VDDR transitions must occur two FSTCLK cycles after the

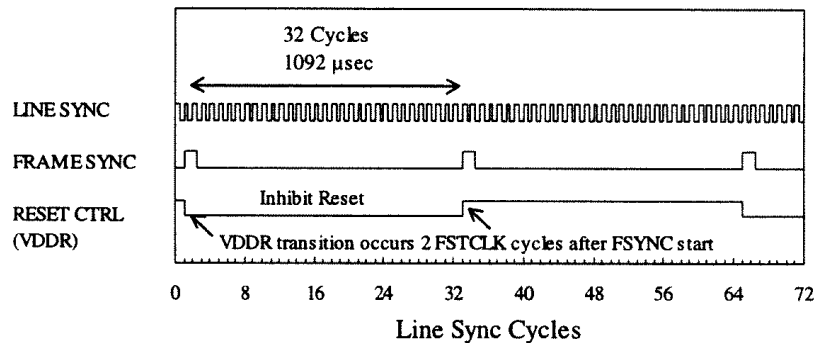


Figure 6. Array timing with reset control for burst mode. Reset is inhibited when the reset MOSFET drain voltage, VDDR, is low.

rising transition of FSYNC. The array is clocked continuously and VDDR held low to inhibit reset for some number of array-reads during which the charge in the array builds up. For the example in Figure 6, reset is inhibited for just one read.

Figure 7 shows the signal processor timing. Each signal processor board serves two channels with separate amplifiers and A/D's and shared digital coadder. Each FSTCLK transition advances the array multiplexer one block to a new set of pixels. The analog signal in the figure represents the transition from one pixel to the next with a time constant of the array output source follower and cable capacitance plus any additional selectable filtering on the board. The track-and-hold hold and A/D convert begin toward the end of the pixel sample time. The two A/D outputs are then sequentially selected and coadded into the coadder memory. The shading shows the timing path for processing one pixel.

Figure 8 shows the timing of the array read in burst mode with chopping. The chopper external reference signal is derived from the camera timing as shown. The array is read continuously during the chop cycle. In this example, the read time is 1.092 msec and the chop frequency 10 Hz. Each box in all but the last line of the figure represents a single read of the full array.

At the first read-coadd, the array is reset and the coadder output for each channel is written to a separate FIFO memory. For the next six reads (a 6.5 msec chop-wait), the array is reset but the coadder output is not used. A minimum of one chop-wait read is required to prevent a pixel integration from being partially in each of two chop positions. For the next eight reads, the array is not reset so the charge integrates on the integrating capacitor. At the following read, the array is reset and the coadder output is written to the coadder memory. The process repeats for a total of four frames coadded for one chop half-cycle when the coadder output is again written to the

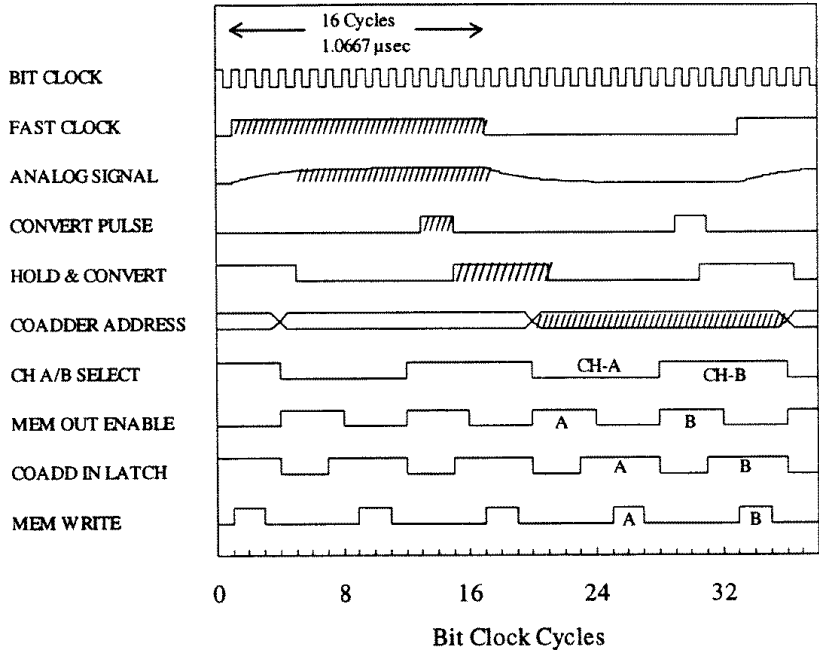


Figure 7. Signal processor pixel timing. There are two channels per board with each channel having its own A/D converter. The two channels share a digital coadder and coadder memory. At the last memory write of a coadd sequence the data is directed to a FIFO memory and the coadder memory locations are zeroed. The A/D convert and coadder memory write are triggered at the trailing edge of the timing pulse.

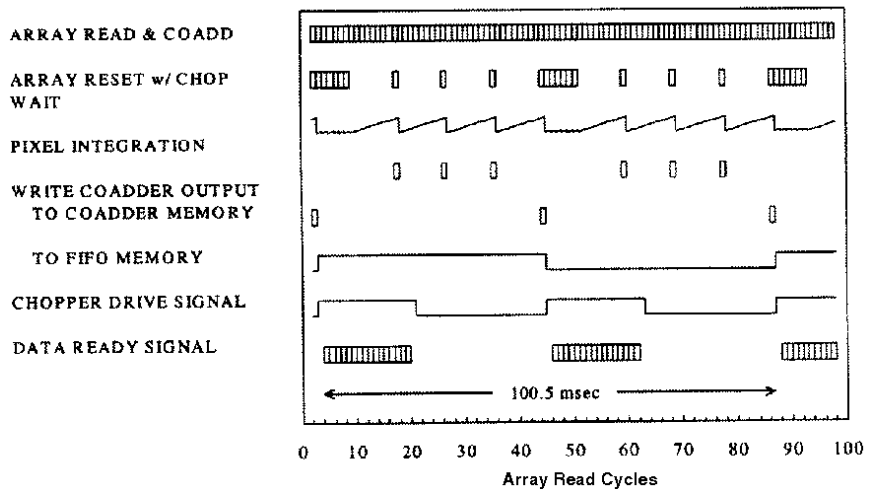


Figure 8. Array read timing with chopping. In this example, the array is continuously reading and coadding at 1.092 msec per array-read. See text for explanation.

FIFO memory. The data-ready signal informs the PC computer that a co-image is ready and the image is read successively from each of the 16 FIFO's to the digital signal processor in the PC, taking about 17 msec for the data transfer while the next chop half-cycle is taking place.

The array is always fully read out. But a selected portion of the array can be coadded and sent to the dsp in order to take and store co-images at a faster rate. In a special "ultra-fast" mode it is possible to acquire and store a set of 800 1/2 x 1/2 array grab co-images at 80 images/second or 3000 1/4 x 1/4 array images at 300/second.

4. CAMERA AND ARRAY PERFORMANCE

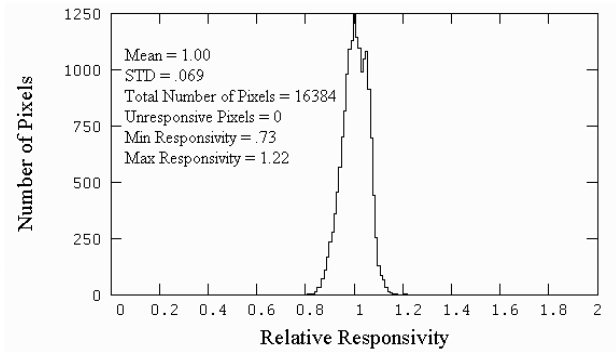


Figure 9. Histogram of HF-16 relative responsivity. This was obtained by taking the difference of images obtained On the dome and on the sky at the IRTF at a wavelength of 7.9 μm . It includes variations due to different channel amplifier gains and differing optics throughput over the array.

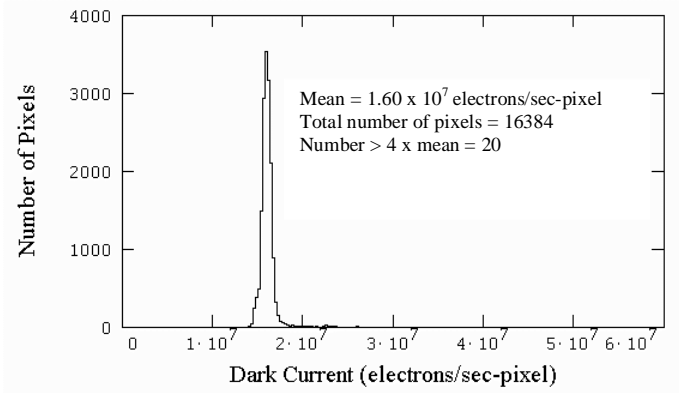


Figure 10. Histogram of HF-16 array dark current

Figure 9 shows a histogram of the HF-16, SN A9-38, relative responsivity. In this remarkable array, all 16384 pixels are responsive. The standard deviation is 6.9% of the mean.

Figure 10 shows a histogram of the dark current. This is very high with a mean of 1.6×10^7 electrons/sec-pixel with 20 pixels with dark current more than 4 times the mean. . This effectively limits on-chip integration time (frame time) to less than 100 msec with up to 20 pixels not useful because they are out of the linear range.. The usual frame times for our various filters run from 2.2 msec to 50 msec. The conversion from A/D units to electrons is determined by measuring the mean array output in A/D units for two values of flux while monitoring the total array current provided by DETS. This, plus the conversion from preamp input volts to A/D units, also gives the effective integrating capacitance of the unit cell multiplied by the integrating capacitor and output source follower's gains.

Figure 11 gives the noise vs read flux in electrons. This is obtained in the laboratory in chop mode at 10 hz. That is, with the array staring at room temperature radiation and running at 20 co-images/second, pairs are differenced for statistical analysis and display. This removes offsets and drift. The noise is taken to be the standard deviation of the pixel values over the array scaled to a single frame (on-chip integration). The theoretical fit to the data is used to determine the read-

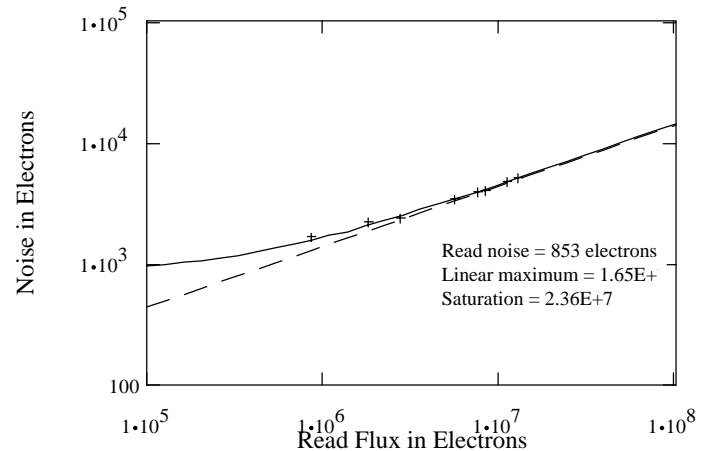


Figure 11. Noise vs read flux in electrons. The + are measured data; the solid line a theoretical fit with read noise and βG as parameters; and the dashed line for the shot noise only.

plus-system noise and the detector gain-times-dispersion (βG). The system noise (mostly A/D toggling noise) and read noise were separately determined by carrying out the noise measurements at two different preamplifier gains. The contribution of the system noise has been removed from the noise shown in figure 11.

Figure 12 shows the array linearity and saturation for 16 pixels representing all channels and all parts of the array. The individual frame times have been scaled to make the low level flux slopes equal to the mean slope to compensate for different dark currents and photon responsivity. The saturation levels and non-linearity are equal for each pixel since these depend on MOSFET and bias, rather than detector, characteristics. The vertical axis at the left gives the well level in electrons. The axis at the right gives the corresponding shot noise. The graph indicates the levels for read noise, for shot noise equal to three times the read noise, and for the non-linear change in slope. The useful dynamic range of the array, between the latter two, is a factor of 4.8.

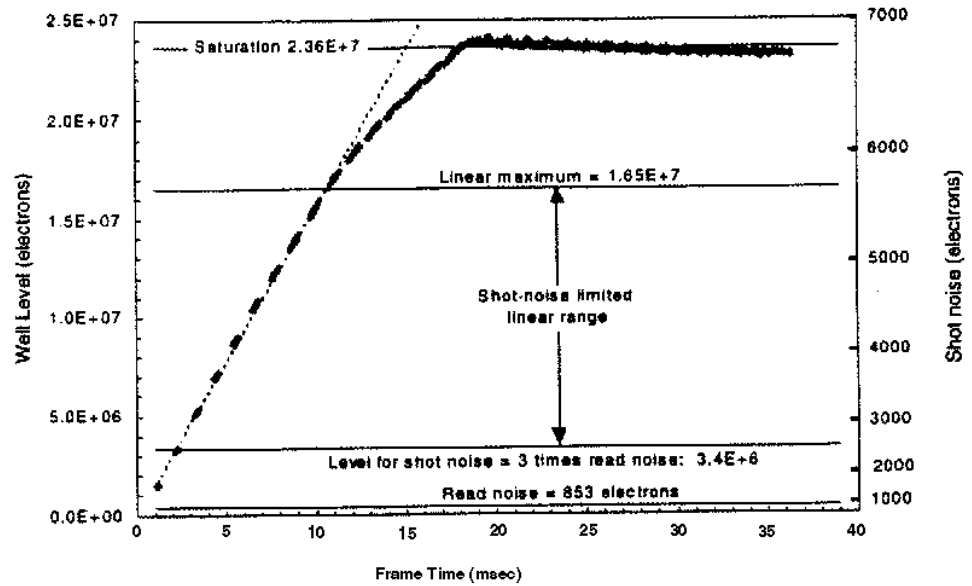


Figure 12. HF-16 linearity and saturation. The data are from 16 pixels, one from each channel chosen from different array columns and rows so that half are from the array upper part and half from the lower part. The well level is relative to the blanked-off array to remove the effect of zero voltage levels and offsets. The individual frame times have been scaled to make the low level flux slopes equal to the mean slope to compensate for different dark currents and photon responsivity. The useful dynamic range is that for which the array is linear and shot-noise limited.

Si:As BIB detectors exhibit a current-dependent excess low frequency noise (ELFN). This noise in some ways mimics shot noise. Subsequent to fabrication of our array, Rockwell reported substantial reduction in this noise (Stapelbroek, *et. al.*, 1995). In our HF-16, as the frequency decreases, the noise increases smoothly from the high frequency value to approximately 2.5 times this value. The change occurs over about a factor of 10 in frequency and has a mid-point which increases in frequency as the detector current increases. Figure 13 gives a plot of the excess low frequency noise vs

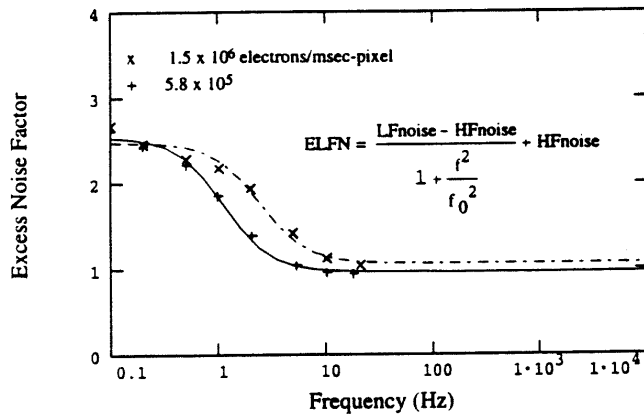


Figure 13. HF-16 excess low frequency noise (ELFN) vs frequency for two flux levels. The equation for the best fit is empirically determined.

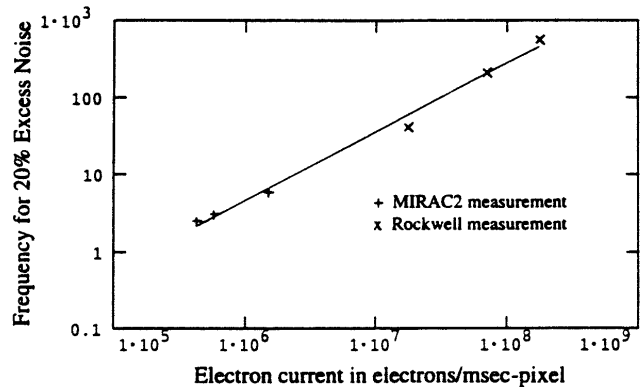


Figure 14. Frequency for 20% excess low frequency noise vs electron flux.

Table 4 HF16 Array, SN A9-38, and MIRAC2 System Properties at 11.7 μm

Array temperature	5.0	K
Detector substrate bias	3.0	V
Detector bias	2.0	V
Read time	1.1	msec
Transimpedance, array output/input	.096	$\mu\text{V}/\text{electron}$
Transfer, preamp input to A/D output	.305	mV/digital unit
Transfer, array input to A/D output	3191	electrons/digital unit
System (A/D toggle) rms noise at A/D	.41	digital units
referred to preamp input	.125	mv
Array single read rms read noise		
array output	.082	mv
array input	853	electrons
Array electron gain times dispersion (βG)	1.96	
Array saturation level	2.29	Volts
	2.36×10^7	electrons
	7400	digital units
Linear range	1.65×10^7	electrons
	5170	digital units
Array background for	3.4×10^6	electrons
BLIP noise = 3 x (read)	1065	digital units

frequency for two values of detector current with data points and best fit curves. The noise at various frequencies was determined by the method described for Figure 11. Figure 13 gives a plot of the frequency for 20% excess low frequency noise vs detector electron current for both MIRAC2 and Rockwell data.

Table 4 gives a number of measured properties for our HF-16. We have not measured the responsivity (quantum efficiency times gain, ηG) of the array at our operating temperature of 5K so we cannot give this, or, using our value of βG , a derived

Table 5 MIRAC2 Background, Sensitivity, and Noise, IRTF 3-m Telescope

Wave Length (μm)	Diffraction FWHM (arcsec)	Frame time (msec)	Backgnd		Noise 1 sigma in 1 minute		
			per pixel (Digital Units)	Sensitivity (Jy/Unit)	Surface Brightness ($\text{mJy}/\text{arcsec}^2$)	Point Source (mJy)	(mag)
2.2	0.16	70	635	.035	5.9	5.5	12.6
3.8	0.27	70	1470	.029	6.5	6.6	11.4
4.8	0.34	70	2320	.057	16	17	9.9
7.9	0.56	50	2710	.40	204	270	5.9
8.8	0.62	35	2530	.059	25	34	7.9
9.8	0.69	20	3210	.11	38	58	7.1
10.3	0.73	20	2750	.082	27	42	7.4
11.7	0.83	20	2550	.080	25	43	7.1
12.5	0.88	20	3200	.071	25	44	6.9
10.6 N	0.75	6.6	3700	.050	11	17	8.2
17.4	1.23	39	3160	1.8	890	2090	2.0
17.8	1.26	31					
18	1.27	4.4	3700	.75	160	390	3.8
20.6	1.46	8.7	3000	2.0	456	1230	2.2
CVF 8.8	0.62	70	1200				
CVF 10.3	0.73	70	1460				
CVF 13.5	0.95	35	2590				

value of the quantum efficiency divided by the dispersion (η/β). β G has been measured by Rockwell at an array temperature of 12K to be 0.70. They estimate that the value at 5K should be about one-half of this value.

Table 5 gives the performance of MIRAC2 at the NASA IRTF with the following settings: magnification, .41 (IRTF pixel .34 arcsec); bandwidth, .71 μ sec; burst mode; read time, 2.2 msec. The noise is for chop-nod, source in one beam, one minute total time except for 2.2 and 3.8 μ m which are chop only. The point source noise is determined from the surface brightness noise by assuming 1/2 of the signal appears in a disk of the root-sum-square of the diffraction FWHM and seeing FWHM (taken to be .5 arcsec). For the Steward Observatory 2.3-m, UKIRT 3.8-m, and MMT 6.6-m telescopes the sensitivity in Jy/unit should be multiplied 1.7, .64, and .46, respectively and the noise in mJy/arcsec² by 1.3, .8, and .46, respectively.

Figure 15 is an illustration of the MIRAC2 display. The display consists of nine areas: top, command line; 2nd line, run status bar; next 5 lines, observing parameters; center graphic, array image with compass directions at the upper right; left graphic, FWHM plot, right graphic, magnified image; lower right graphic, source radial profile; next 9 lines, image statistics; and bottom 2 lines, observing and display status. The displayed image can be processed by adding or subtracting chop and nod images and applying a mask, flat field, and gain map as desired.

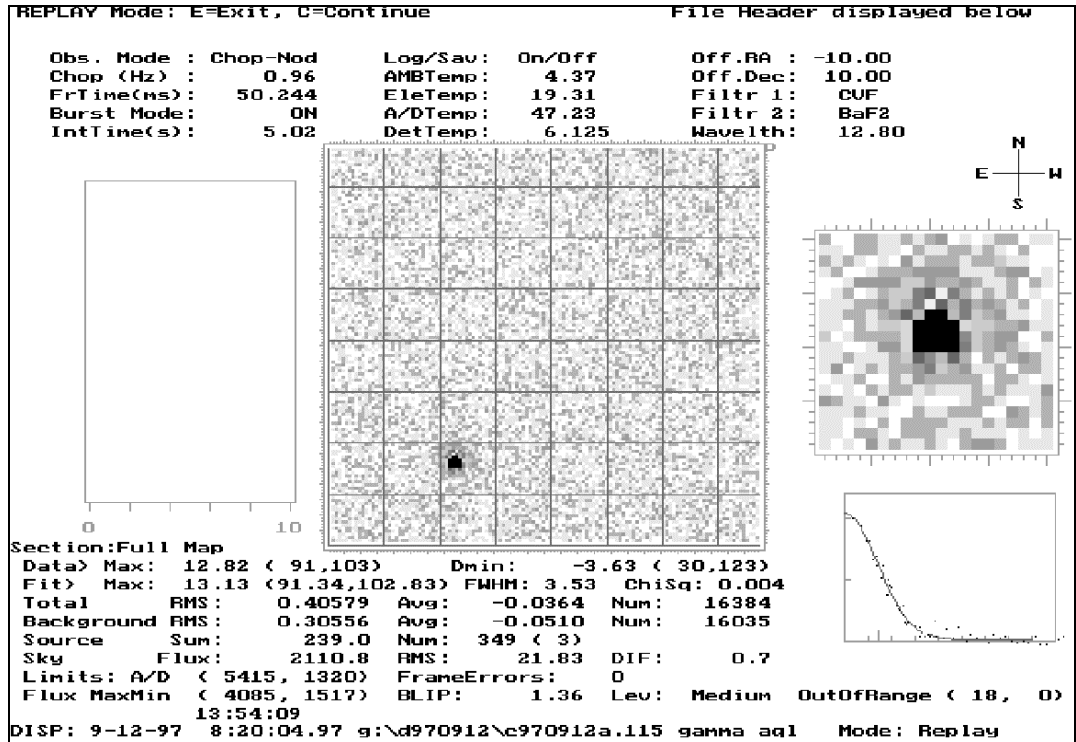


Figure 15. MIRAC2 Main Screen showing an IRTF image of Gamma Aql at a CVF wavelength of 12.8 μ m.

Also given are the sky flux and the ratio of the measured STD to that predicted for shot noise only for the measured background.

Figure 16 illustrates the MIRAC2 observation of the SL9-Jupiter collision at the NASA IRTF in July 21, 1994.

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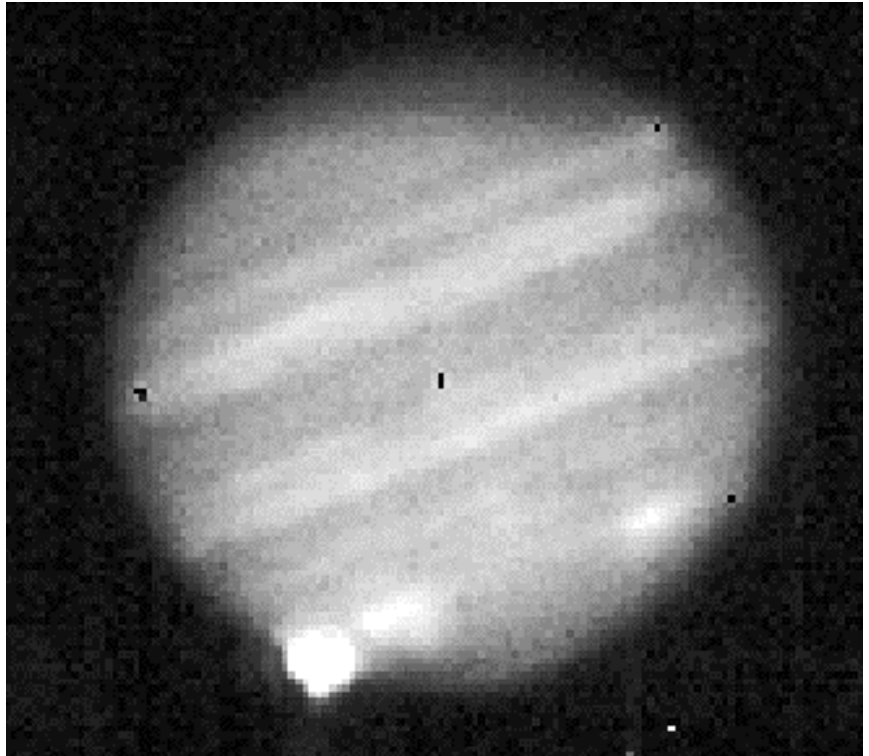


Figure 16. MIRAC2 10.3 μ m image of Jupiter during the impact of the comet, Shoemaker-Levy 9, R fragment at the IRTF July 21, 1994. This is displayed as a raw image with no pixel masking or flat fielding. The only processing is the subtraction of an off-source sky image taken by beam switching with the telescope. The pixel size is .4 arcsec.

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For further information:

email: whoffmann@as.arizona.edu; MIRAC web page: <http://cfa-www.harvard.edu/~jhora/mirac/mirac.html>